Amendments to the Specification:

Please replace the paragraphs beginning on page 5 lines 6-28 with the following rewritten paragraphs:

-- A digital data stream ds transmitted with the aid of a transmission protocol is passed to one input ET of the phase/frequency control device PLL and is passed on to an input ~~EF~~ EF1 of a sampling flipflop AFF. In the exemplary embodiment, it is assumed that the data stream ds is transmitted in accordance with the Synchronous Digital Hierarchy SDH. The Synchronous Digital Hierarchy is based on synchronous transmission of user information using synchronous transport modules (also referred to as STM) with a standard structure. The basic transport module is the STM-1 frame, with a data transmission rate of 155 Mbit/s. Each STM-1 frame includes a matrix of 9 rows each having 270 data octets. The frame has a repetition frequency of 125 µs, and the transmission is carried out at a bit rate of 155.520 Mbit/s. The STM-1 frame is inserted into a payload and an overhead, with the first 9 octets in all 9 rows containing the overhead, and the remaining columns containing the payload. The overhead contains information which is required to operate SDH systems, and these are also referred to as section overheads (SOH) and are transported in the SOH areas of the overhead. The SOH areas contain, for example, the A1 and A2 bytes, which are known to those skilled in the art, and which each represent frame identification information.

The data input ET of the phase/frequency control device PLL is at the same time connected to a first input EP of a discriminator unit DE. A reference signal f_{Ref} at a reference frequency is passed to a second input ~~EF~~ EF2 of the discriminator unit DE. The discriminator unit DE is functionally subdivided into two components, a phase discriminator PD and a frequency window discriminator FD, each indicated by a rectangle with a dashed outline. --

Please replace the paragraph beginning on page 9 line 23 with the following rewritten paragraphs:

-- As already explained, the phase locked loop which is arranged in the phase/frequency control device PLL is matched to the data transmission rate of the incoming digital data stream ds via the control loop control information PLL_WORD1 stored in the register unit REG. By way of example, the transmission of appropriate control information ~~si2,3~~si2, si3 via the control lines SL2 and SL3 sets the controllable frequency dividers T1, T2 such that the frequency of the signal delivered from the voltage controlled oscillator VCO is divided as appropriate for matching of the optimum operating point of the phase discriminator PD and of the frequency window discriminator FD. Additional control information, in this case si4, transmitted via the fourth control line SL4 is used to provide any possibly required presetting or switching of the voltage controlled oscillator VCO. According to one alternative embodiment of the circuit arrangement, a number of voltage controlled oscillators VCO can be arranged in the phase/frequency control device PLL, in which case one voltage controlled oscillator VCO, which is matched to the data transmission rate of the incoming digital data stream ds, in each can case be selected with the aid of the fourth control signal si4. --